REMARKS

Claims 1-11 are all the claims pending in the present application. In summary, the Examiner substantially maintains the previous prior art rejections of the pending claims. Specifically, claims 1, 3, 6, 9 and 10 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Blais et al (U.S. Patent No. 7,065,743) in view of Sauntry et al (U.S. Patent No. 6,349,344). Claims 2, 4, 5, 8 and 11 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Blais in view of Sauntry, and further in view of Rodriguez et al (U.S. Patent No. 6,725,241).

§103(a) Rejections (Blais / Sauntry) - Claims 1, 3, 6, 9 and 10

Claims 1, 3, 6, 9 and 10 are rejected essentially based on the same reasons set forth in the previous Office Action, except the Examiner adds a few new arguments in the *Response to Arguments* section of the Office Action.

With respect to independent claim 1, Applicants previously argued that the applied references, either alone or in combination, do not disclose or suggest at least, "a second memory unit for storing the runtime data, which have been loaded into the first memory unit in the accessible state, in a form of images," "wherein said first memory unit and said second memory unit are separate," and "a runtime data search unit for loading the runtime data, which have been stored in the second memory unit in the form of images, into the first memory unit upon the request of the class loader unit," as recited in claim 1. *See paragraph bridging pages 6 and 7 of Office Action.* In response, the Examiner alleges:

> In regard to the argument "that Blais does not disclose a second memory unit and a separate first memory unit", (emphasis in original - See response, page 7, 1st paragraph), the Examiner

> respectfully disagrees. It should be noted that the plain language of the claim limitation separate is interpreted by the Examiner, as distinguishable (emphasis added). As such, the cache 126 is clearly distinguishable from the main memory 120, processor 110, and class processing mechanism 129. Even arguably, if the Applicant is intending to imply that the memories are different physical memory chips, the disclosure of Blais would at least have suggested to one of ordinary skill in the art, at the time the invention was made, to look to the known methods of class loading in a java virtual machine (i.e., See col. 2, lines 35-47 + col. 2, lines 63-67 + col. 5, lines 57-61) to further enable Blais' objective of increasing the performance of Java Virtual Machines (JVM) by eliminating needless processing of Java classes which have already been processed (see col. 2, lines 65-67).

In response, Applicants maintain that Fig. 1 shows that the data 121, operating system 122, class file 123, cache 126, cache entry 127, and class processing mechanism all constitute the main memory 120. Therefore, each of the above listed items are clearly not separate or distinguishable from the main memory 120. Applicants acknowledge that the processor 110 is, in fact, separate from the main memory, however, the cache 126/127 clearly is not. See Fig. 1 of Blais. Therefore, the cache entry 127, which the Examiner believes corresponds to the claimed second memory unit, is clearly not separate from the maim memory 120, which the Examiner believes corresponds to the claimed first memory unit. At least based on the foregoing as well as previously submitted arguments, Applicants submit that claim 1 is patentably distinguishable over the applied references, either alone or in combination.

Applicants submit that independent claim 6 is patentable at least based on reasons similar to those set forth above with respect to claim 1.

Further, the Examiner alleges:

> Even arguably, the old and well known methods of implementing a JVM by loading data from a first memory into a second memory

> would have been obvious. As evidence of the above statement and further support of the Examiner's arguments, see Rodriguez, Fig. 2 and col. 2, lines 12-48, wherein a JVM includes a class loader subsystem 202, for loading classes into the first memory (runtime data areas) 204 from a second memory. Rodriguez expressly defines the run-time data areas to "represent the organization of memory needed by JVM 200 to execute a program (emphasis added, col. 4, lines 27-28). Even if that memory is a reference to a different memory, it is still a distinguishable or separate (second) memory. Accordingly, the rejection is maintained as addressed herein-above and below in the claim rejections, in light of the instant argument.

In response, Applicants respectfully request that the Examiner issue a new non-Final Office Action citing Rodriguez as an applied reference if the Examiner wishes to rely on the teachings of Rodriguez to support the claim rejections of claims 1, 3, 6, 9, or 10. Applicants would gladly respond to any rejections of these claims that are based on Rodriguez once this reference is officially applied against claims 1, 3, 6, 9, or 10.

Applicants submit that dependent claims 3, 9, and 10 are patentable at least by virtue of their respective dependencies from independent claims 1 and 6.

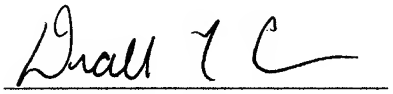
§103(a) Rejections (Blais/Sauntry/Rodriguez) - Claims 2, 4, 5, 8 and 11

Applicants submit that dependent claims 2, 4, 5, 8 and 11 are patentable at least by virtue of their respective dependencies from independent claims 1 and 6. Rodriguez does not make up for the deficiencies of the other applied references.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Diallo T. Crenshaw
Registration No. 52,778

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: October 12, 2007